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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,615	01/08/2004	Stuart W. Hayes	016295.1509 (DC-05592)	6328

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,615	HAYES ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities:

Claim 1, line 15, "the electrical trace" should be changed to - - an electrical trace - - for proper antecedence basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selna (U.S. Patent 5,640,048) in view of Teshome et al. (U.S. Patent 6,236,572).

As to claim 16, Selna discloses a BGA package for IC as shown in figure 3 comprising:

a circuit board (100) having an electrical trace (8, 10, the elements 8 and 10 formed on to and bottom surfaces of the board 100)) and voltage and ground planes (260, 200, column 7, lines 56-59) formed on first and second layers, the electrical trace (8, 10, see figure 3) routed over a portion of the circuit board,

the electrical trace (8, 10) including first and second paths (8C, 10C) such that the first path references the ground plane and the second path references the voltage plane whereby the first path is substantially similar to the second path; and *the first path electrically coupled to the second path at each of the ends of the paths (**the electrical connection of the first and second paths defined by conductors filled in Vss vias 6C**).*

Selna does not disclose the circuit board (100) having a processor and a memory chip communicatively coupled to.

Teshome et al. teaches a computer system as shown in figures 1-2 comprising a memory (24, 26) communicatively coupled to a processor (12), and communicatively coupled to a printed multilayer circuit board (28). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Teshome employed in the package of Selna in order to storing data, and facilitate and control data signals for the computer.

As to claim 17, Selna discloses the first path (8C) is located at a distance from the ground plane (200) that is substantially equal to the distance the second path (10C) is located from the voltage plane (260).

As to claim 18, Selna discloses the ground and voltage planes (200, 260) are symmetrically oriented about the circuit board.

As to claim 19, Selna discloses the first and second paths (8C, 10C) and the second path are symmetrically oriented about the circuit board.

As to claim 20, Selna discloses in figure 3 the first path and the ground plane are a mirror image of the second path and the voltage plane.

Response to Arguments

4. Applicant's arguments with respect to claims 16-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

Selna (in figure 3) does not indicate that "either of the signal paths 8C and 10C reference either the Vdd plane 260 and Vss plane 200"

Examiner disagrees because:

First, the element 8C and 10C are not signal paths, the paths 8C and 10C are ground paths (note: the signal path is never connected to ground or power, it only connected to another signal path, for example, element 8B).

Second, the paths 8C and 10C are formed on top and bottom of the Vdd and Vss plane (260, 200), therefore, they do reference either of the planes to provide ground connection between a chip (12) and a board (18).

Thus, examiner believes the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
May 11, 2006.